REMARKS

Claims 1-7, 9, 11-19, 21-51 are pending in the present application. Claims 8, 10 and 20 have been cancelled. Claims 45-51 are newly added hereby.

Claim Rejection under 35 U.S.C. §102

(1) Claims 1, 8, 10, 12, 20, 22, 24, 26, 28, 31, 34 and 37 were rejected under 35 U.S.C. §102(b) as being anticipated by *Kazuhiro* (JP 2000-269219A).

As described in claims 1, 12, 22 and 45, the semiconductor device according to the present invention has a feature that the device includes a groove-shaped via-hole having a pattern bent at a right angle, a hole-shaped via-hole, a first buried conductor filled in the groove-shaped via-hole, and a second buried conductor buried in a hole-shaped via-hole, and the relationship between a width of the groove-shaped via-hole and a width of the hole-shaped via-hole is defined in a prescribed range. In claims 1 and 22, the width of the groove-shaped via-hole is set to 20-140% of the width of the hole-shaped via-hole. In claims 12 and 45, the width of the groove-shaped via-hole is set to not more than the width of the hole-shaped via-hole.

The pattern size shift of the width of the groove-shaped via-hole at the lithography step tends to be larger than that of the width of the hole-shaped via-hole according to the proximity effect. Even though the widths of the groove-shaped via-hole and the hole-shaped via-hole on the reticle are set to the same size, the finished size of the width of the groove-shaped via-hole becomes larger than the finished size of the width of the hole-shaped via-hole. Especially, the

width of the groove-shaped via-hole is more widened at the bent portion. As the result, defective filling of the groove-shaped via-hole appears, and the crack and/or peeling of the inter-layer insulating film caused by the defective filling occurs (see, e.g., page 14, line l2 to page 19, line 13 of the present specification).

According to the present invention, considering the size shift by the proximity effect, the width of the groove-shaped via-hole on the reticle is set such that the finished size of the width of the grooved-shaped via-hole becomes the prescribed range as claimed. Due to this feature of the present invention, defective filling of the first buried conductor is prevented, and the cracking and/or peeling of the inter-layer insulating film are also prevented. Also, steps on the first buried conductor plug are reduced, so that the step does not affect the upper interconnection layers and inter-layer insulating layers. Accordingly, defective contact with the upper interconnection layer and the problems in forming films are prevented, and as a result, water resistance and interconnection reliability of the semiconductor device are improved.

As described above, it is important for improving the water resistance and the interconnection reliability that the relationship between the width of the grooved-shaped via-hole and the width of the hole-shaped via-hole is set within the prescribed range as claimed.

On the other hand, *Kazuhiro* discloses, in e.g., FIGs. 1 and 2, the semiconductor device including the contact grooves 23A, 24B and 25B having patterns bent at a right angle, and the conductor walls 23B, 24C and 25C filled respectively in the contact grooves 23A, 24B and 25B. However, *Kazuhiro* does not teach or suggest the hole-shaped via-hole, or the relationship

between the width of the groove-shaped via-hole and the width of the hole-shaped via-hole. Even if the hole-shaped via-hole is added to the semiconductor device of *Kazuhiro*, the relationship between the width of the groove-shaped via-hole and the width of the hole-shaped via-hole cannot be set in the prescribed range as claimed based on the disclosure of *Kazuhiro*.

For at least these reasons, claims 1, 12, 22 and 45 patentably distinguish over *Kazuhiro*. Claims 8, 10 and 20 have been cancelled. Claims 24, 26, 28, 31, 34 and 37, directly or indirectly depending from claim 1, also patentably distinguish over *Kazuhiro* for at least the same reasons.

(2) Claims 1, 8, 10, 12, 20, 22, 24, 26, 28, 31, 34 and 37 are rejected under 35 U.S.C. §102(b) as being anticipated by *Kazumi* (JP 2003-086590A).

Kazumi discloses in, e.g., FIG. 1 and 2, the semiconductor device including the annular grooves and the annular walls 11, 15, 19, 22 buried in the annular grooves. *Kazumi* also discloses the annular groove 30 and the via-hole 70 formed in the insulating film 18 in, e.g., FIG. 4(a), and the annular wall 19 filled in the annular groove 30 and the via-plug 69 filled in the via-hole 70 in, e.g., FIG. 5(b). However, *Kazumi* does not teach or suggest the relationship between the width of the groove-shaped via-hole and the width of the hole-shaped via-hole.

For at least these reasons, claims 1, 12, 22 and 45 patentably distinguish over *Kazuhiro*. Claims 8, 10 and 20 have been cancelled. Claims 24, 26, 28, 31, 34 and 37, directly or

indirectly depending from claim 1, also patentably distinguish over *Kazuhiro* for at least the same reasons.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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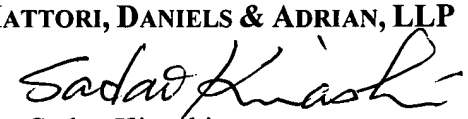

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